



FIG. 1

STRUCTURE OF THE FIRST EMBODIMENT

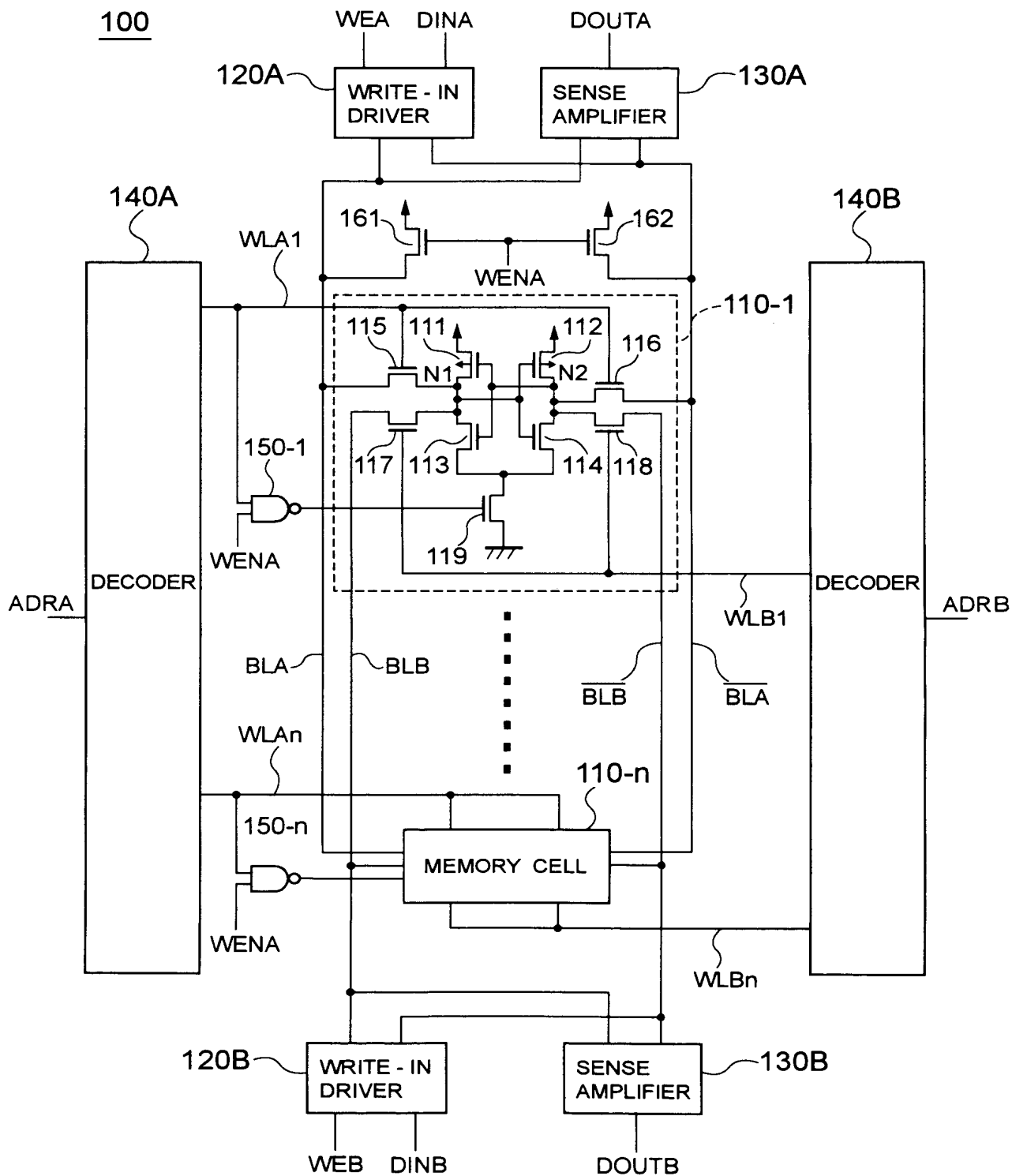


FIG. 2

OPERATION OF THE FIRST EMBODIMENT

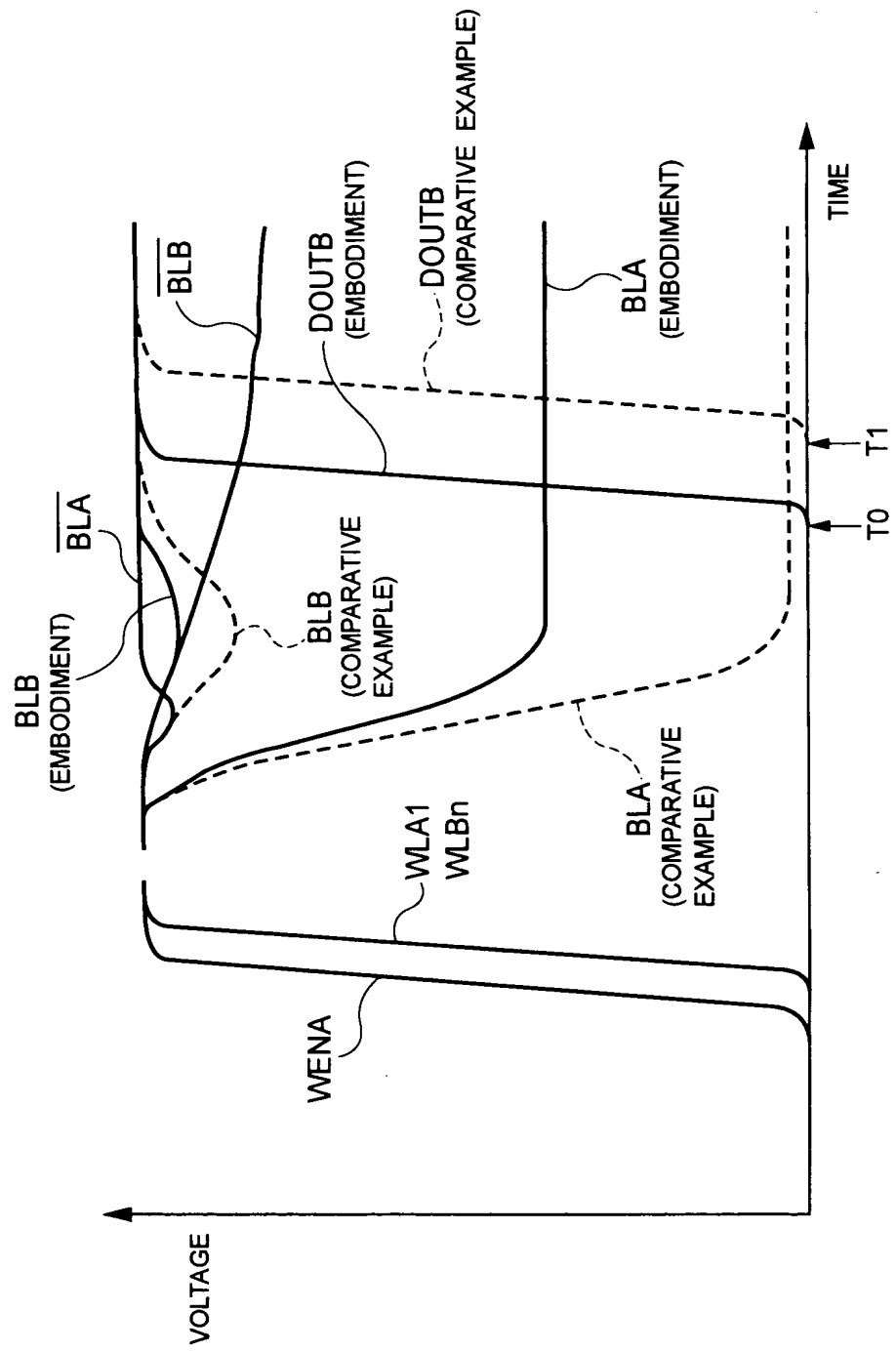


FIG. 3

STRUCTURE OF MULTI-PORT SEMICONDUCTOR
MEMORY FOR COMPARISON

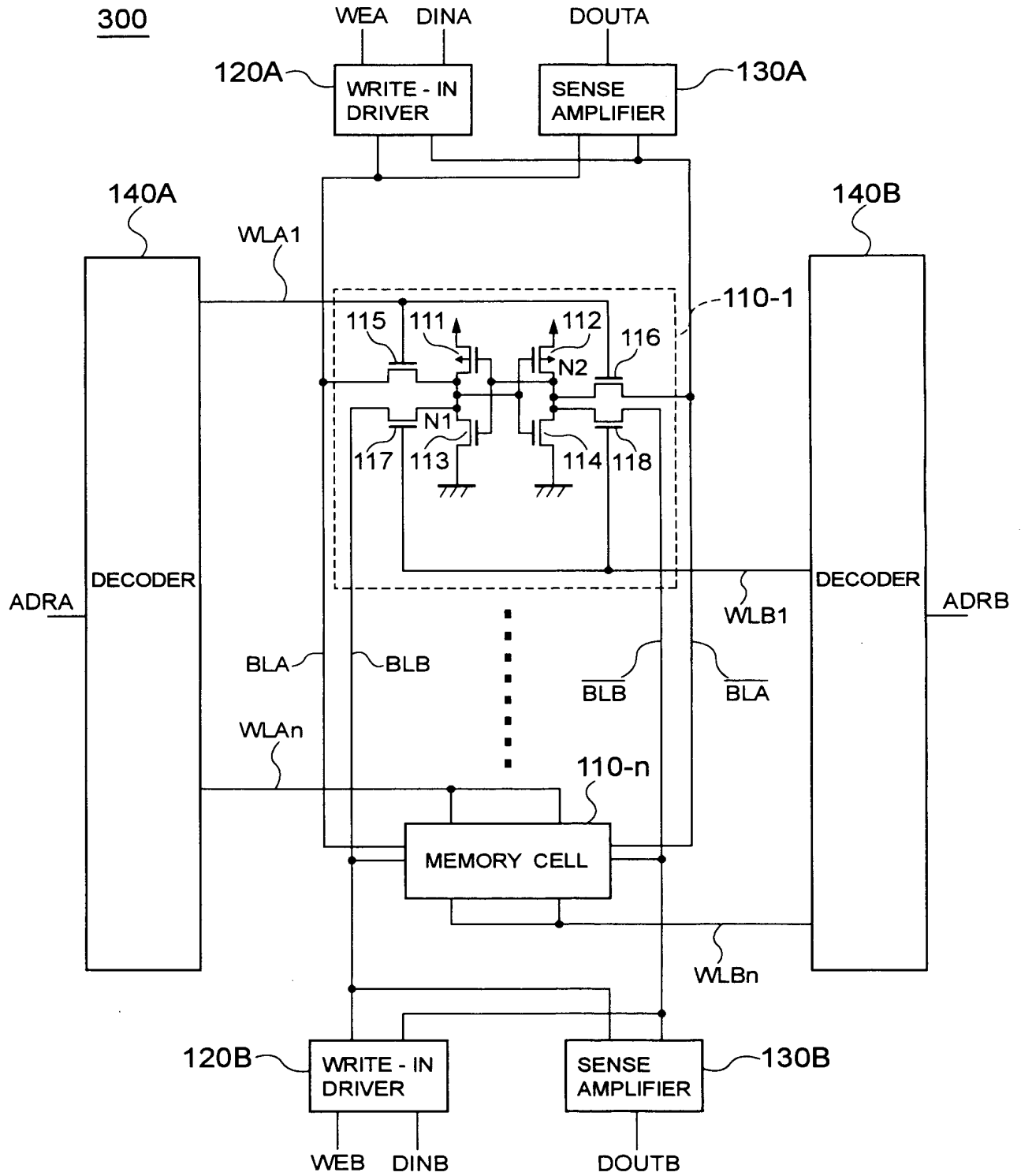


FIG. 4

STRUCTURE OF THE SECOND EMBODIMENT

